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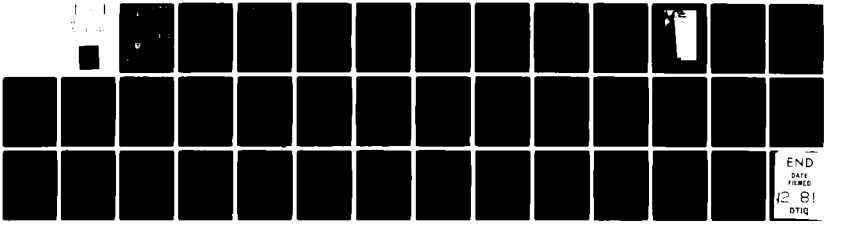

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TECHNICAL REPORT RE-81-6

SIGNAL ANALYSIS VAN HARDWARE OPERATION GENERAL DESCRIPTION (VOLUME I)

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December 1981

U.S. ARMY MISSILE COMMAND
Redstone Arsenal, Alabama 35898

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Signal Analysis Van
Process Control System
Data Acquisition
Satellite Bus

20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Signal Analysis Van is comprised of general-purpose high-speed programmable data acquisition hardware housed within a 45-foot commercial semitrailer equipped with a RF shielded enclosure. The Signal Analysis Van is capable of capturing and storing several channels of high-bandwidth, high-dynamic-range signals typical of many high-performance radar and missile-seeker systems. Programmable features permit fast and accurate interfacing with a variety of sensor systems alleviating the necessity for hardware redesign and modifications as new requirements are generated.

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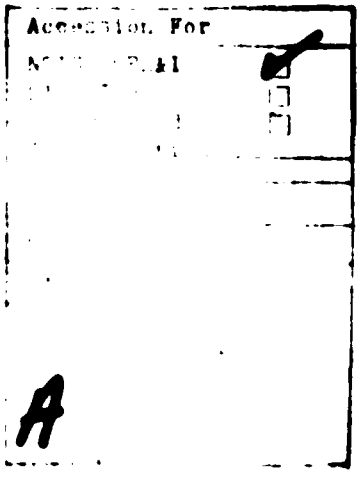

I. INTRODUCTION

A prevailing need among many developmental sensor systems is the requirement for acquisition and recording of high resolution signals for subsequent playback and off-line processing. To satisfy this requirement, a mobile Signal Analysis Van (SAV) has been developed by the Advanced Sensors Directorate to facilitate data collection, decrease system development time, and provide a vehicle with which to demonstrate operational feasibility. During development of the SAV, several different aspects of acquisition and recording of high-bandwidth, high-dynamic-range signals, as encountered in radar systems, were considered. Several different designs were formulated and a configuration chosen which would provide the maximum performance and operational compatibility with a variety of radar and missile-seeker systems. The extent to which the SAV can be utilized in the current configuration for acquiring and processing data is dependent upon several parameters. Evaluation of a particular requirement may necessitate the addition or modification of hardware in order to provide the best possible support during test and evaluation; however, it is expected that with the current electronics, the SAV will be capable of handling a very wide variety of data storage and processing functions. These include real-time recording of quadrature radar video and selected digital signals at various points in the radar processing and control channels. Availability of this type of data will assist in the evaluation of radar performance along with providing valuable radar clutter data for analyses and as real-time inputs to signal processing simulation for algorithm development.

II. SIGNAL ANALYSIS VAN APPLICATION

The expanded hardware capability offered by the SAV makes it applicable to a wide variety of sensor/seeker devices. The modular design approach and high-speed digital components provide the flexibility required for fast, accurate data acquisition. Data outputs are stored on computer-compatible tapes in formats which can be readily analyzed by most processing systems. Design architecture will allow future growth to advanced data storage mediums and special test support hardware.

III. RADAR SYSTEMS APPLICATION

The predominant factor in development of the SAV was the eventual application in test and evaluation of ground-based radar systems. Consequently, the SAV was designed to provide maximum performance and flexibility in this or similar applications. Particular interest lay in the ability to capture radar video and processed information for complete characterization of terrain clutter, radar tracking, and signal processing functions.

Specific capabilities of the current SAV hardware are directly dependent on the particular operational parameters of the radar

under test and performance characteristics to be evaluated; however, it is often desirable to acquire data for a particular range and azimuth window during each revolution of the radar. The extent of this window is limited by either the size of a temporary SAV buffer memory or the combination radar revolution time and buffer memory dump rate. For an azimuth window

$$A \geq 360 - \frac{360\ (T)}{T_R} \tag{1}$$

where

T = Time to dump W_m words in buffer memory (sec)

T_R = Radar revolution time (sec)

The maximum allowable range cell window size is

$$R = \frac{(360)\ T_D}{(A)\ (P)} - \frac{T_D}{(P)} \tag{2}$$

An equivalent azimuth window can be found, given a fixed range window size, by

$$A = \frac{(360)\ T_D}{(R)\ (P) + T_D} \tag{3}$$

If an azimuth window size were selected such that

$$A \leq 360 - \frac{(360)\ T}{T_R}$$

then the allowable range cell window size is computed from the relationship

$$R = \frac{(360)\ Wm}{(A)\ (P)\ (T_R)} \tag{4}$$

with an equivalent azimuth window of

$$A = \frac{(360)\ Wm}{(R)\,(P)\,(T_R)} \qquad (5)$$

where

R = number of range CELLS in window

A = Azimuth size in degrees

P = Radar pulse repetition frequency

T_D = Memory dump rate in words/sec

Wm = Total number of buffer memory words

If we assume

T_R = 3 sec

T = 2 sec

Wm = 262,144 words

P = 700 pulses/sec

then from equation (1)

$$360 - \frac{360\ (2)}{3} = 120°$$

Therefore, if an azimuth window of greater than 120 degrees is desired, then equations (2) and (3) should be used. Azimuth windows less than 120 degrees would necessitate the use of equations (4) and (5) to compute the range or azimuth windows. Assuming a fixed azimuth window of 100 degrees, then, from equation (4), we compute

$$R = \frac{(360)\,(262,144)}{(100)\,(700)\,(3)} = 449.38 \text{ words/pulse}$$

Thus, an azimuth/range window of 100 degrees and 449 range cells could be acquired and dumped for every revolution of the radar.

(It should be noted that the unit of R is words/pulse and that each word could contain more than one channel of radar information.) If an azimuth window greater than 120 degrees were computed from equation (5), assuming a fixed range cell window size, then equations (2) and (3) would be used rather than equations (4) and (5). Specific values for parameters relating to the memory size and dump rate for the SAV electronics are given in the SAV hardware operation's Volume IV, Buffer Memory System.

IV. DESCRIPTION OF SAV SUPPORT SYSTEMS

A. Trailer

The various SAV support systems, including electric power generator, air-conditioning, and RF shielded enclosure are housed within a standard 45-foot commercial semitrailer, as shown in Figures 1 and 2. The trailer has been especially equipped with underslung storage, generator, air-conditioner compartments, and a power control room. Other salient features of the SAV trailer include the following:

- Exterior floodlighting for work area illumination
- Exterior utility power outlets
- Roof access steps
- Reinforced roof catwalk
- External AC power inputs to van

B. Shielded Enclosure

To aid in personnel safety and the prevention of equipment malfunction in high RF energy fields, a shielded enclosure was installed within the semitrailer shell. This enclosure is 30 feet in length and is constructed of 16-gauge welded-steel panels. Signal access panels and two RF screened windows are also provided. During normal operation when RF shielding requirements are minimal, the RF screened windows are covered with glass panels to allow operator visibility; however, during test where greater RF attenuation is desired, these glass panels can be removed and replaced with solid steel panels. In this mode of operation, the enclosure is rated at 60 dB of attenuation at a center frequency of 40 GHz. All signals entering the shielded enclosure are filtered in order to maintain proper RF shielding.

C. Generator and Air-conditioner Units

The SAV is provided with external power entrance connectors when commercial power is available; however, in the event commercial power is unavailable, a 100-kw, 3-phase, 4-wire, 60-Hz

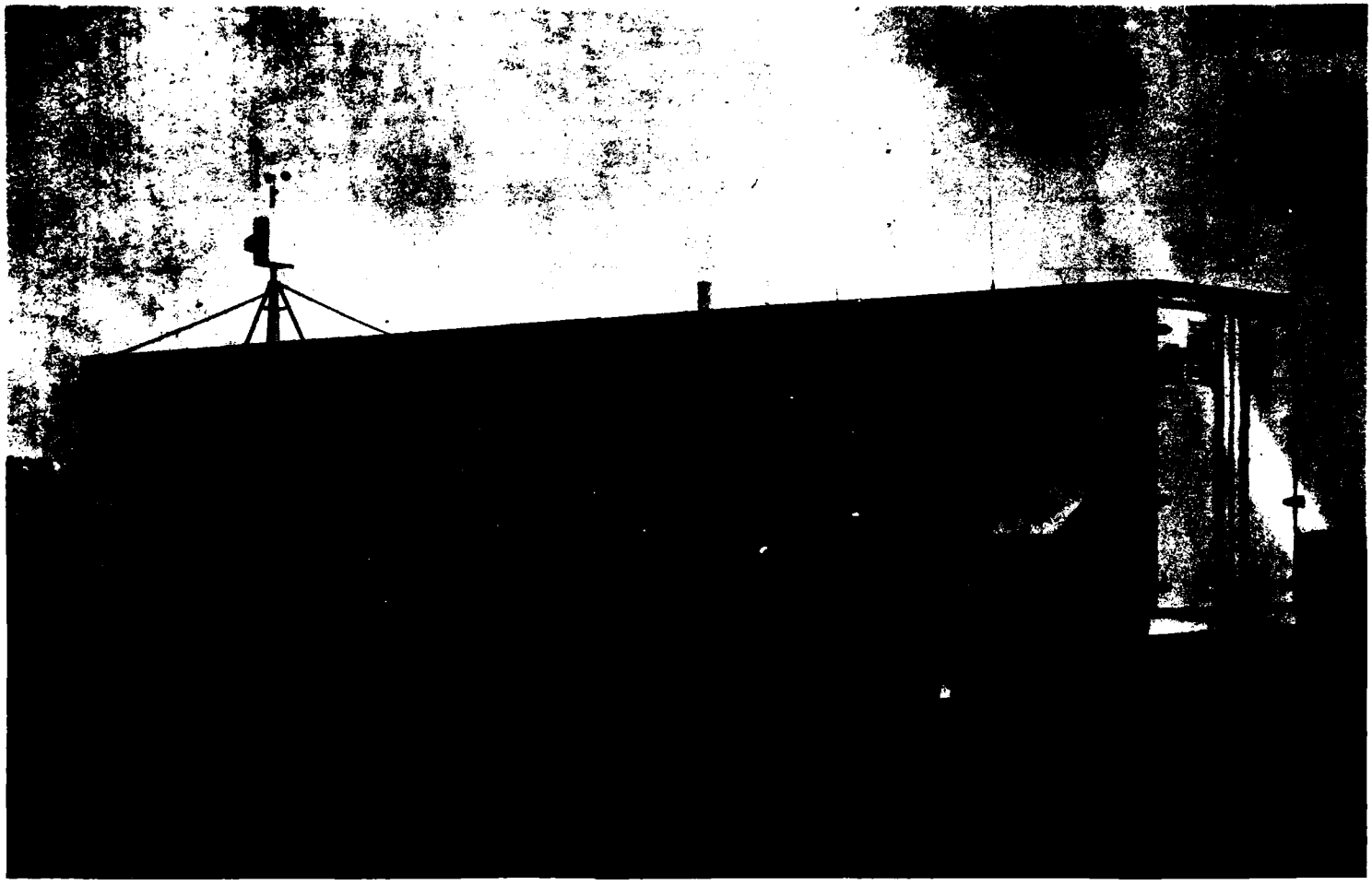

Figure 1. Standard 45-foot commercial semitrailer.

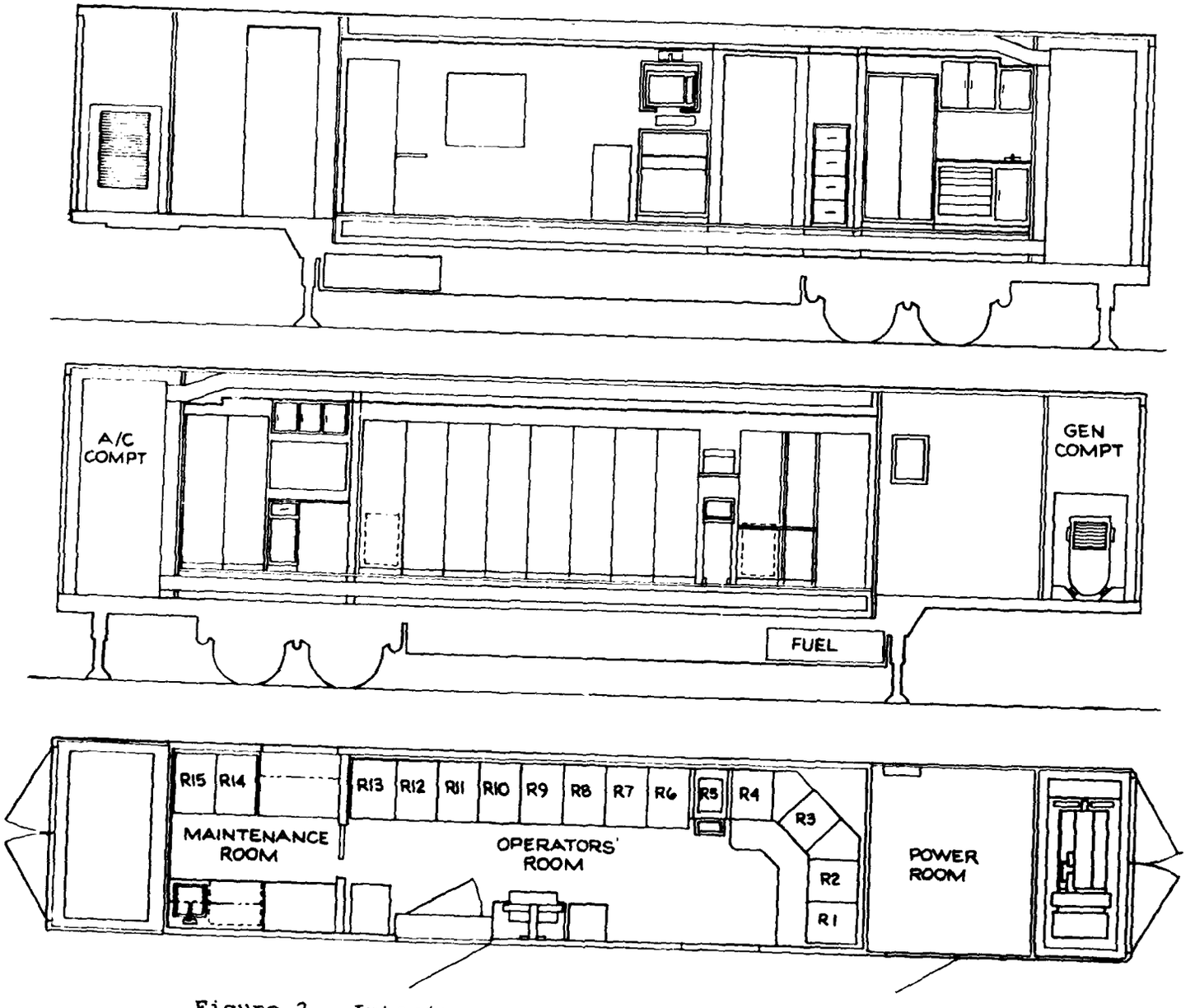

Figure 2. Interior views of Signal Analysis Van.

diesel generator is provided. The generator is equipped with remote start/stop and engine monitor capability located inside the SAV operations room. The generator is fueled with a 200-gallon tank located in the lower forward portion of the van.

An environmental control system is furnished to provide cooling for rack-mounted equipment and heating in low ambient temperatures, as well as to provide cooling, heating, ventilation, and dehumidification for the personnel. It consists of two independently operable air-conditioners mounted in the same enclosure and located at the rear of the van. The units are rated at 45,000 Btu cooling and 14 kW heating for personnel, and 89,000 Btu and 7 kW heating for equipment. This enables the units to maintain a 75°F temperature with outside ambient temperatures ranging from -10°F to 115°F. Thermostants and AC power controls are located inside the SAV operations room.

D. Power Room

The SAV power room located next to the generator provides the control and distribution point for all AC and DC power. This room also serves as storage for a special electronic rack and other miscellaneous hardware.

E. Operations and Maintenance Areas

The operations and maintenance rooms located within the RF shielded enclosure contain all the data acquisition and control electronics along with ancillary test equipment, mobile telephone, and spare parts inventory. Standard equipment racks and a raised access floor are provided for equipment mounting and cable routing. The maintenance area is also equipped with a work bench and cold water wash basin.

V. CONTROL AND DATA ACQUISITION SYSTEM DESCRIPTION

The SAV data acquisition and control system is subdivided into two major categories as shown in Figure 3. The general-purpose processing and control system (PCS), configured around standard commercially available computer and peripherals, provides command, control, and display functions. Together with the high-speed, general-purpose data acquisition hardware (HDAS), these units provide the capability for acquiring and recording high bandwidth information in a digital format.

A. Processing and Control System

The Processing and Control System (PCS) illustrated in Figure 4 utilizes a 16-bit mini-computer, built by Digital Equipment Corporation, equipped with several standard input/output (I/O) peripherals and control hardware options. The PDP-11/10 computer was selected because of its availability and compatibility with existing in-house computer analysis systems, enabling development

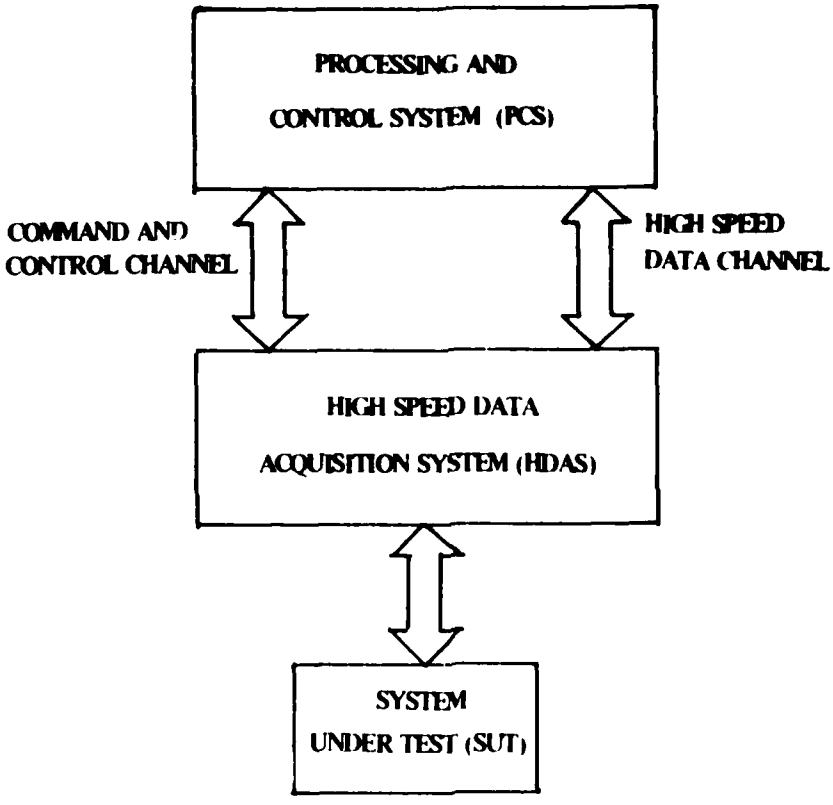

Figure 3. Control and data acquisition system block diagram.

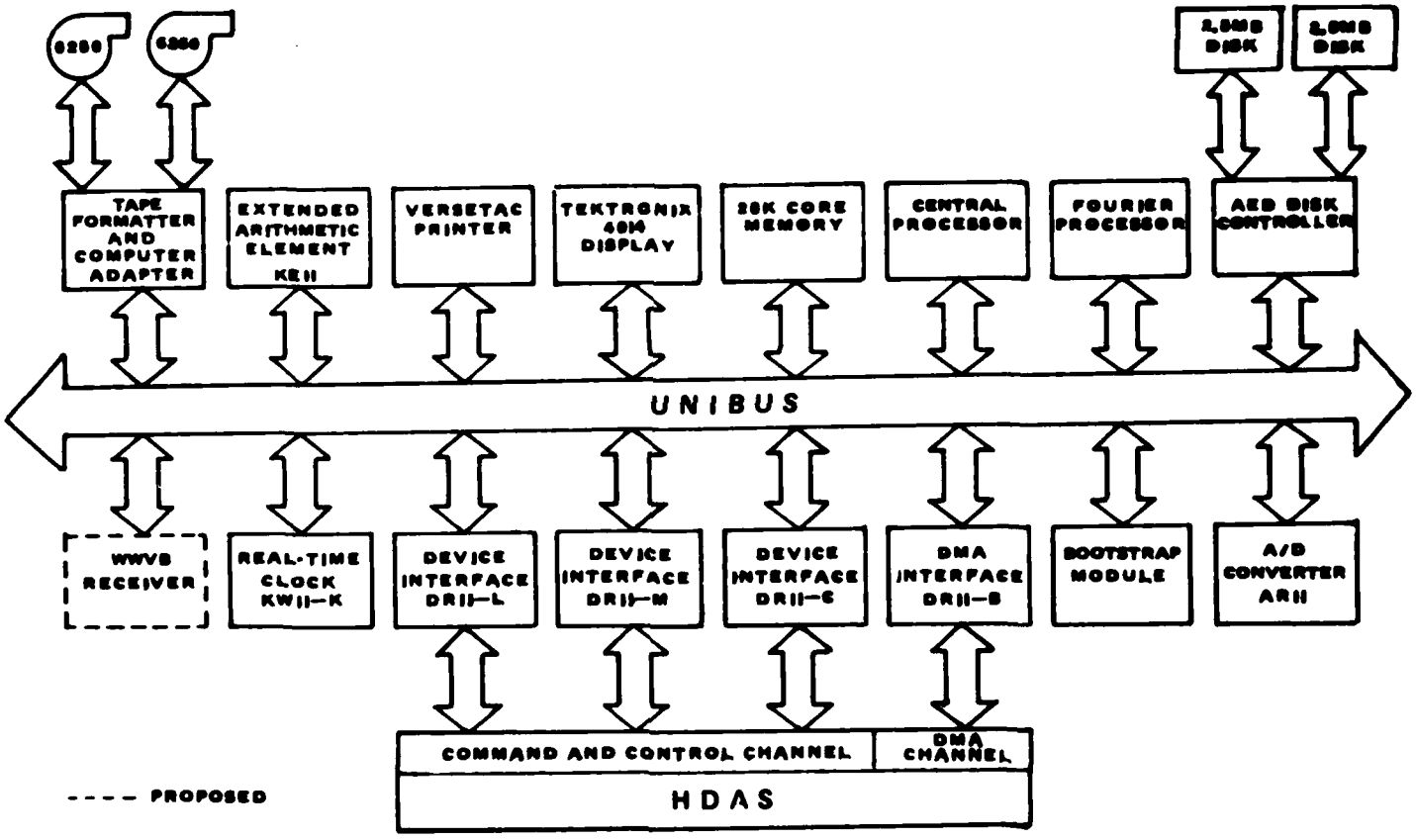

Figure 4. Processing and control system block diagram.

and transfer of software between these systems. It has a very rich instruction set, extensive software support, a full range of peripheral devices and special hardware options. The following are some of the characteristics of the PDP-11 equipment:

- Processor and Bus Architecture

  - 16-bit word (two 8-bit bytes) direct addressing of 32K 16-bit words

  - Word and byte processing

  - Asynchronous bus operation

  - Automatic priority interrupt

  - Vectored interrupts

  - Eight general registers

- Instruction Set

  - Over 400 instructions

  - 12 addressing modes

  - Compatibility with other PDP-11 family computers

Further discussion of the PDP-11, including system configuration, bus operation, and instruction, can be found in PDP-11/10/34 processor handbook.

1. Supporting Peripherals. The various hardware options and ancillary equipment contained in the system are as follow:

- 28K words of 900-nsec core memory
- Bootstrap module
- Dual Diablo disk drives and controller
- Tektronic 4014 display and keyboard
- Versatec line printer and hard copy
- Dual magnetic tape drives and controller
- Extended arithmetic element
- 16-channel analog-to-digital converter
- Programmable real-time clock

- General device interfaces
- Fourier processor

2. Description of Peripherals/Options

a. Core memory. The PDP-11 CPU is equipped with 28K words of core memory with an access time of 375 nsec typical and 980 nsec cycle time. One 16K-word memory module is located within the CPU mounting box, while the remaining 12K-word memory module is contained in a separate expension chassis.

b. Bootstrap module. The CPU is equipped with a general-purpose program loader. This module contains bootstrap loaders programmed for most frequently used PDP-11 devices, such as disk or magnetic tape. Provision is also made for bootstrap operation via external push-button switches.

c. Disk storage. Two Diablo disk drives and an Advanced Engineering Development (AED) controller are included in the system providing a total storage capacity of 5.0 megabytes. Average latency time for disk access is 20 ms with a 781-kHz bit transfer rate. Unit 0 of the two drives contains a locked-in cartridge and requires a technician to make an exchange. Most of the system type software, including the RT-11 operating system, is resident on this disk. Unit 1 is a removable platter drive and is used primarily for application software development.

d. Computer display terminal. The computer display terminal is a Tektronix-type 4014-1 permitting inputs through an integral keyboard and providing a display (alphanumeric or graphic) of computer output data. It is interfaced to the PDP-11/10 with a KL11 serial-line-interface operating at 19K baud. The unit is configured for graphics tablet interface for operation with interactive graphics software. Hard copy printouts of the 4014 display are produced using the Versatec line printer in a hard-copy mode. This is discussed in the next section.

e. Line printer. A Versatec model 1110A printer/plotter is provided for listing output and hard copy functions associated with the 4014 display terminal. Printing is accomplished using an electrostatic writing method enabling fast, quiet, and compact operation. Hardware design permits compatibility with existing line printer software currently used in the operating system. Versaplot plotting software is also available to permit high quality plots to be generated by the Versatec printer. The unit is also equipped with a plug-compatible link between Tektronix 4014 and the printer unit. A display hard copy, initiated from the 4014, will cause immediate copy of the display. If a copy function is initiated during an output operation to the printer, the hard copy process will begin only after the current computer direction transmission is completed. Detailed specifications for the 1110A are given in Appendix A.

f. Magnetic tape transports. Two high-performance magnetic tape transports, an associated formatter and a PDP-11 I/O attachment feature, are supplied with the SAV computer system. Each unit is capable of operation at 125 in./sec at either 1600PE or 6250GCR bytes/in. Auto-load features enhance the drive flexibility and functions with Easy Load I or Easy Load II tape seals. The tape formatter provides the control necessary to operate up to four tape units. It is electrically located between the host computer I/O controller and the tape units. The formatter provides control for selection, timing, encoding, decoding, data transfer, and status/error conditions for the attached tape units. In addition, the formatter provides error correction. Detailed performance characteristics for both the drives and formatter are supplied in Appendix B and further information can be obtained from Telex Maintenance Manuals 96A20457 and 96A20421.

The PDP-11 attachment feature contains the circuitry necessary to interface a Telex tape subsystem consisting of a 6850 formatter and up to four 6250 tape drives to a Digital Equipment Corporation PDP-11 computer.

The Telex tape subsystem is functionally equivalent to the Digital Equipment Corporation TU10 tape subsystem, except for the higher data rates supported by the Telex formatter and tape drives. The tape drives may consist of any combination of 45, 75, 100, 125 in./sec models operating in NRZI-PE or GCR-PE modes. All tape drivers attached to the formatter must include the manual density select option. Modifications were made to the existing magnetic tape handler to provide operational compatibility with the current operating system software.

g. Extended Arithmetic Element (KE11). The KE11 Extended Arithmetic Element device is attached to the PCS bus and executes hardware arithmetic operations at rates much greater than the central processor. It performs signed integer multiply (16-bit × 16-bit), signed integer divide (32-bit/16-bit), signed normalize, and multiple shifts either with sign extension or by filling with zeros. Typical multiply and divide speeds are 6.6 μsec and 7.4 μsec, respectively.

h. Analog-to-digital (A/D) converter (AR11). The AR11 is a one-module real-time analog subsystem that interfaces with the PDP-11 family of computers via a "hex" small peripheral controller slot. The AR11 includes a 16-channel, 10-bit A/D converter with sample-and-hold, a programmable real-time clock with one external input, and a display control with two 10-bit D/A converters. It also includes all the Unibus interfacing logic necessary for control in a small peripheral controller slot, plus a transformer less DC-to-DC converter allowing a power use of only +5 V.

The A/D converter is a 10-bit successive approximation converter, where the data are right-justified in offset binary. It is controlled by the A/D status register. An A/D

conversion may be started in three ways: under program control, an overflow of the real-time clock, or on an external input. These methods give the system the flexibility to serve in most applications requiring data acquisition. The user can choose one of 16 single-ended channels of analog input under control of the A/D status register. In addition, one can program for either unipolar or bipolar input. When a conversion is complete, a flag is set and, if the A/D interrupt is enabled, the processor will interrupt (vector) to the proper subroutine for data manipulation. The user can run in the interrupt mode or wait for the appearance of the A/D Done flag. The multichannel throughput rate is 30 kHz. A second conversion can be started before the results of the first conversion are read; this overlapping achieves the high throughput. The single-channel throughput rate with clocked or external starts is 35 kHz. Detailed specifications for the AR11 A/D are given in Appendix C. Further information can be found in Digital Equipment Corporation operations manual DEC-11-HARUG-B-D.

i. Real-time clock (KW11-K). The KW11-K is a dual programmable real-time clock option used in PDP-11 Unibus computers. The clock features include the following:

- Clock A
  - 16-bit counter
  - 16-bit programmable preset/buffer register
  - Four modes of operation
  - Two external inputs (Schmitt trigger)
  - Eight clock rates, program selectable
  - Five clock frequencies, crystal controlled for accuracy
  - Synchronous to external events of processor actions
  - Program-compatible with LPSKW
- Clock B
  - 8-bit counter
  - 8-bit programmable preset register
  - Repeated internal mode of operation
  - One external input (Schmitt trigger)

- Seven clock rates, program selectable
- Five clock frequencies, crystal controlled for accuracy

Clock A is a 16-bit programmable real-time clock, which can accurately measure and count intervals of time and events. It can be used for processor synchronization to external events, generate events, such as A/D conversion at programmed intervals, and generate events synchronized to an external event input. Clock A is controlled by the A Status Register, which consists of enables, flags, and mode and rate selections.

Clock A operates in one of four programmable modes: single interval, repeated interval, external event timing, or external event timing from zero base. Clock A can be program selected to operate at one of eight clock rates. The clock can operate from one of five crystal-controlled frequencies (1MHz, 100 kHz, 10 kHz, 1 kHz or 100 Hz), an external (Schmitt Trigger One) input, line frequency or the overflow of Clock B (allowing a further dimension in Clock A input frequency selections).

Clock B is an 8-bit programmable real-time clock which can accurately time intervals or events. It can be used to generate interrupts at programmed intervals, to generate events (such as an A/D conversion) at programmed intervals, or to provide an input frequency to Clock A. Clock B is controlled by the B Status Register which consists of flags, enables, and rate selection. Clock B operates in one mode: repeated interval mode. Clock B can be prgram-selected to operate at one of seven clock rates, one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, or 100 Hz.), line frequency or external (Schmitt Trigger Three) input. Detailed specifications are given in Digital Equipment Corporation manual, EK-KW11-K-OP-001.

j. General device interfaces. There are several general-purpose PCS device interfaces used in the SAV system. Included are a DR11-L two-word input interface, DR11-M two-word output, DR11-C 16-bit I/O, and the DR11-B DMA interface. The DR11-L, M, C are used to construct a slow-speed data link between the High-speed-programmable Data Acquisition System (HDAS) and PCS. The DR11-B DMA is used to provide a fast processor-unassisted transfer of data from the HDAS.

k. Fourier Processor Element (FPE). The FPE is a modular low-cost, high-performance processor for performing Fourier transforms, both direct and inverse, as well as auto and cross power spectrums. The unit is designed to plug into a PDP-11 computer extension mounting box and interface directly to the UNIBUS. For direct and inverse Fourier transforms, the FPE operates on 16-bit two's complement integer data in real or complex form to generate an array of two-word complex integer output points.

The following processing functions can be performed in the FPE unit:

- Real-to-complex direct Fourier transform
- Complex-to-complex direct Fourier transform
- Complex-to real inverse Fourier transform
- Complex-to-complex inverse Fourier transform
- Frequency domain hanning
- Auto spectrum
- Cross spectrum
- Frequency domain averaging of auto- or cross-spectra

B. High-speed Data Acquisition System

The key to overall flexibility and expanded capabilities over existing systems is the High-speed-programmable Data Acquisition System (HDAS). The HDAS is composed of several high-speed elements linked together by a common 32-bit bus, referred to as the Satellite Bus (SB). As illustrated in Figure 5, the current HDAS configuration consists of a Computer to Satellite Bus Interface (CSBI), High-speed Data Formatter (HSDF), a Buffer Memory (BM) and associated Buffer Memory Controller (BMC), Reconfigurable System Interface Unit (RSIU) and associated Analog to Digital Converter Unit(ADCU). General descriptions for each of these units and the Satellite Bus follow; however, more detailed discussion of each of these devices is given in four separate volumes on the SAV hardware operations:

- Volume II - Computer to Satellite Bus Interface
- Volume III - High-speed Data Formatter
- Volume IV - Buffer Memory System
- Volume V - Reconfigurable Systems Interface Unit

1. Satellite Bus. The HDAS Satellite Bus (SB) is a common set of signal lines that connect each of the HDAS devices. Address, data, and control information are transmitted along the 47 lines of the bus. Utilization of high-speed current mode drivers and receivers permits operation at extended bus lengths of up to 275 meters at a 5×10^6, 32-bit word rate. Each of the 47 signal lines comprising the SB are listed in Appendix D. The bus is broken down into two major categories: data and control. All data lines are bi-directional, i.e., they can function as input

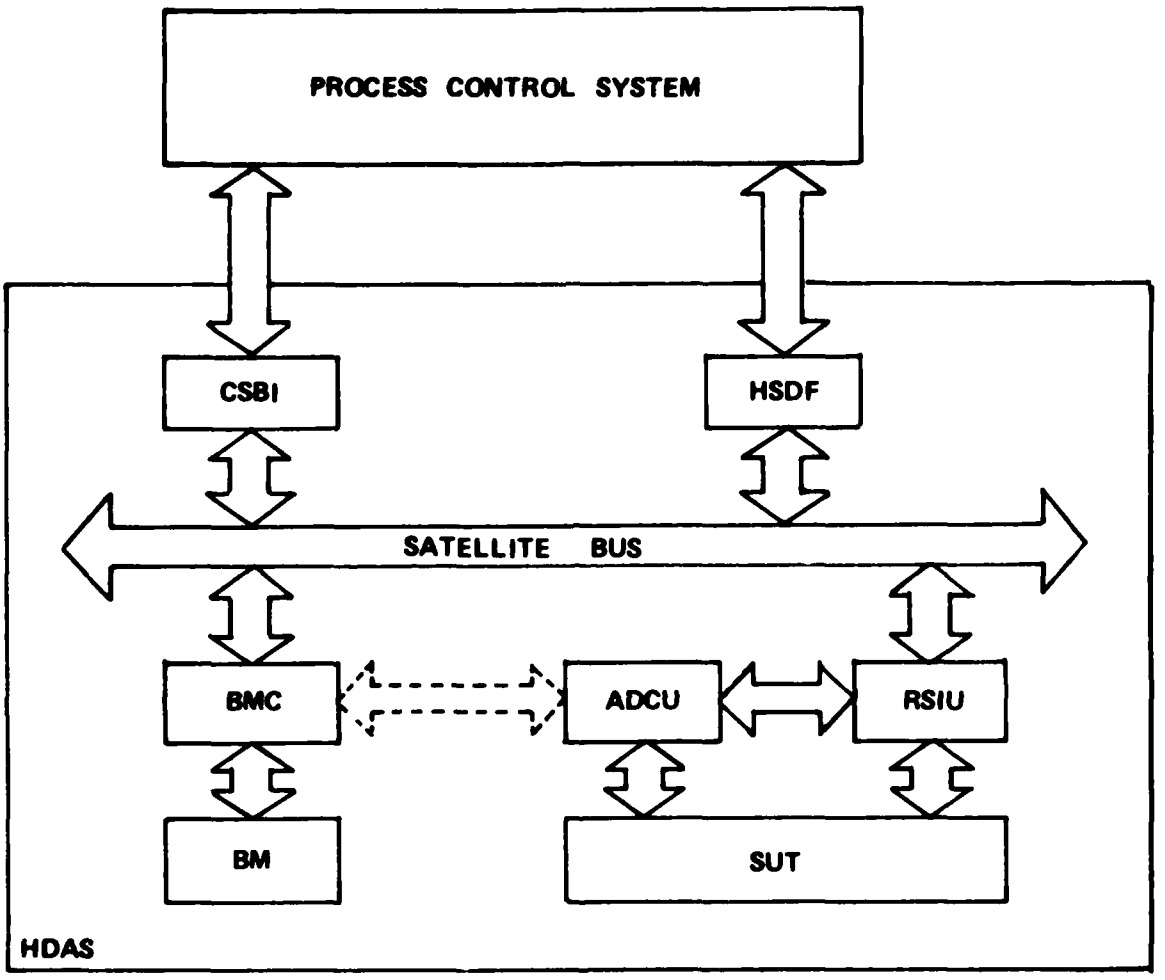

Figure 5. High-speed data acquisition system block diagram.

or output to a particular device. The control signals may be either bi-directional or uni-directional, depending on the particular function.

Communication between devices (usually two) on the bus is in a master/slave relationship. During any bus operation, one device has control of the bus. This device, the bus master, controls data transfer with another device on the bus, referred to as the slave. The bus master has the responsibility of initiating, controlling, and terminating the bus operation. Other devices on the bus not designated as either master or slave are dormant and initiate no operations on the bus. Since the HDAS is a satellite to the process control system (PCS), ultimate control of the satellite bus resides with the PCS. Initialization of HDAS is done from the PCS software. Once the bus devices have been initialized and the master-slave relationships defined, the PCS relinquishes control of the HDAS bus, and data transactions between the master/slave are free to begin. Upon completion or termination of bus operation, control returns to the PCS.

Because the SB was designed specifically for high-speed operation in the HDAS, data transactions generally occur in a burst mode. Once data transfer begins, a predefined set of operations occurs with the master sending data packets upon receipt of a ready status from the slave device. The only exception to this is when the PCS reads or writes to a SB device. Single word transfers occur between the slave device and the Computer-to-Satellite Bus Interface (CSBI).

2. Computer-to-Satellite Bus Interface. The CSBI effectively links the HDAS bus to the PCS bus permitting operation and control of the HDAS hardware via the PCS peripherals and associated software. This device provides a common data control path for initialization of the various SB devices. Interface between the HDAS and the PCS is accomplished using several general-purpose PCS device interfaces and satellite bus hardware.

3. High-Speed Data Formatter. The High-Speed Data Formatter (HSDF) is a slave-only device connected to the SB via standard driver/receiver interface cards. It is also linked to the PCS bus by a standard DR11-B DMA interface. During high-speed data transaction, the HSDF provides the primary path for transfer of data from other HDAS devices to the PCS for processing and/or storage on magnetic tape. Data packets are buffered in the HSDF before being transferred to the PCS, thus providing complete asynchronous operation.

4. Buffer Memory System. The Buffer Memory (BM) and associated controller (BMC) are the key units within the HDAS which provide expended capability for data storage and control. The BM system functions at a maximum rate of 10^7 words per second with 32 bits per word. Within the limits of the BM size, data can be acquired from an external device and stored into the memory for later transfer and storage on a permanent medium. Typical

operation of the system involves transfer of data from one of four BMC input data ports and storage in the high density semi-conductor BM. The BMC is a micro-programmed controller and can be configured with firmware developed and loaded from the PCS.

5. Reconfigurable System Interface Unit. The Reconfigurable System Interface Unit (RSIU) is used to link the system under test to the HDAS. Current design allows the unit to be programmed for various modes of system/SAV operation. The RSIU also provides for custom logic design within the unit to satisfy any unique requirements associated with a particular system. Unallocated control bits provide a means of user programming of the customized logic interface.

6. Analog-to-Digital Converter Unit. The Analog-to-Digital Converter Unit (ADCU) is composed of several high-speed analog-to-digital converter units ranging in speed and size from 9-13 bits at 0-10 MHz. They are designed to perform digitization of various analog signals, i.e., radar video, and interface directly with the RSIU or BM subsystems. The ADCU is equipped with a 16-bit Digital-to-Analog Converter (DAC) under direct control of the PCS. The DAC converter output can be selected for input to each of the A/Ds in the unit. This feature permits calibration and/or operational checks to be performed from the PCS during the course of a test.

7. HDAS Hardware Organization. The HDAS design utilizing a high-speed bus permits flexible organization of units on the bus. Bus extensions of up to 275 meters, operating at 5×10^6 words per second, enable SAV hardware components to be located adjacent to the device or System Under Test (SUT). This means that high-speed HDAS devices, such as the RSIU and BM, can be located next to the SUT to provide maximum performance.

Figures 6 and 7 illustrate some of the various configurations which can be realized with the HDAS. When maximum speed and performance are required, a setup such as illustrated in Figure 6 could be used. Here the RSIU, BM, and BMC are co-located next to the SUT. Digitization and data storage through a special BMC input port occurs at speeds up to 10^7 words per second until the BM word count is satisfied. Data are transferred from the BM to the PCS over the SB at a slower rate and permanently stored on magnetic tape. During these operations, the RSIU provides control commands to the ADCI to initiate data acquisition functions. Another commonly used mode is illustrated in Figure 7. Here the RSIU and ADCU are located next to the SUT while the BM and BMC are inside the SAV. This mode requires less hardware next to the SUT, but limits the overall system capability to the maximum bus speed. Data transfers are directed by the RSIU (bus master), with digital information passing down the bus to either the BM or the HSDF (bus slave), depending on speed. For speeds less than 200×10^3 words per second (16-bit), data can be sent directly to the HSDF, thence to the PCS in a continuous manner. When data are dumped to the BM, a BM full signal redirects bus operation to empty the BM

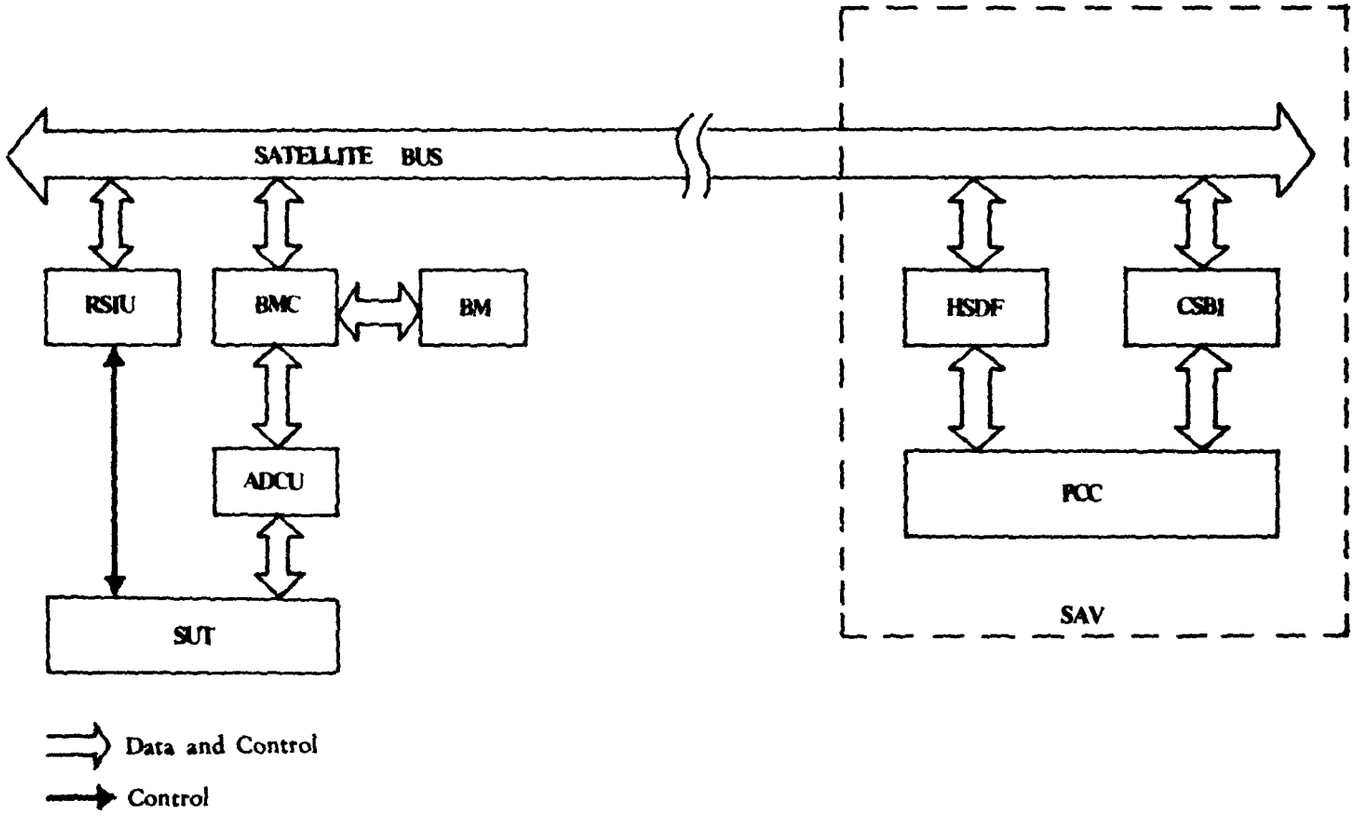

Figure 6. HDAS configuration 1.

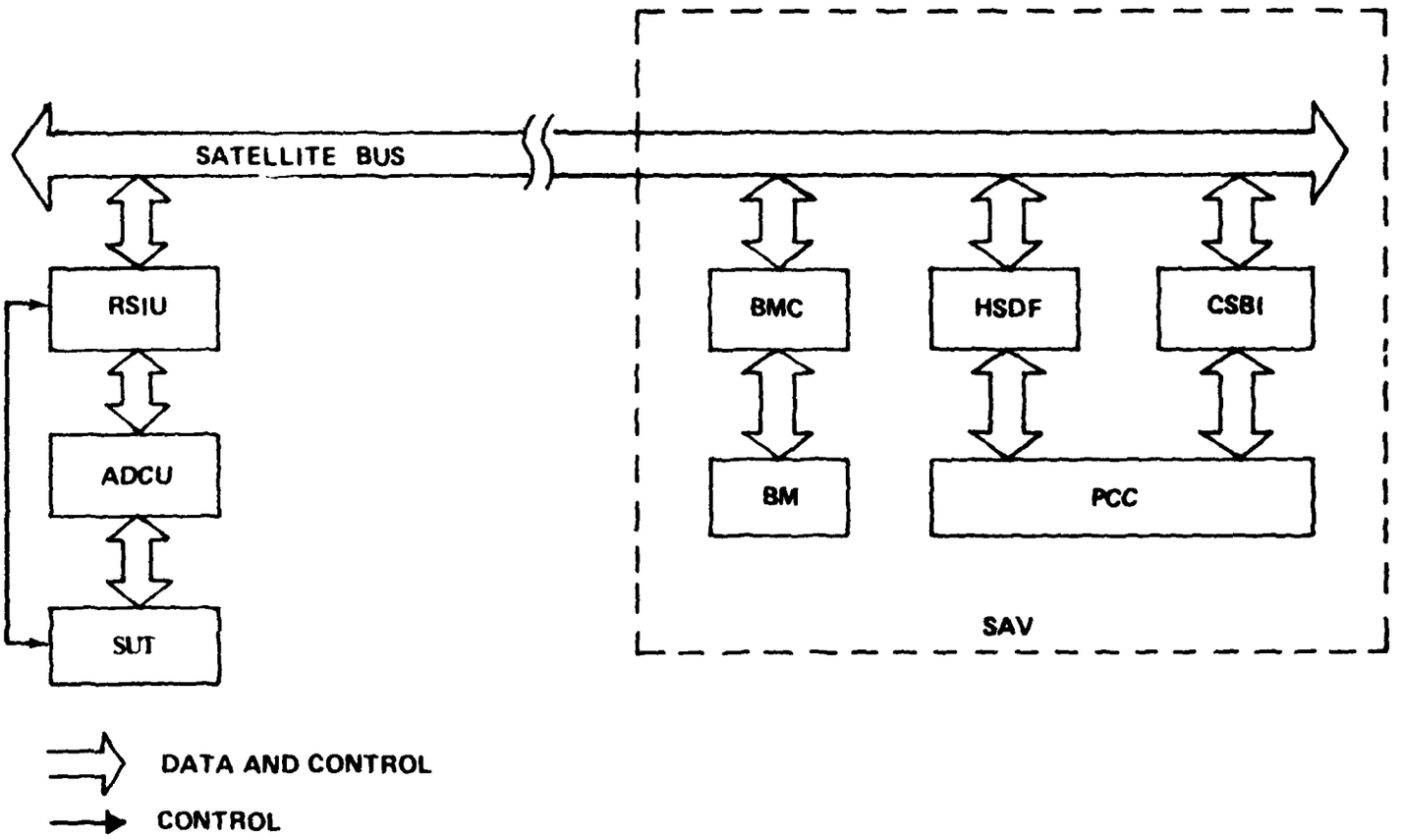

Figure 7. HDAS configuration 2.

through the HSDF and finally to the PCS tape peripherals. Specific discussions of SB operation in various configurations are presented in Volume II: HDAS Hardware Operations.

VI. HARDWARE MAINTENANCE

The Hardware Maintenance Volumes I-V contain detailed circuit schematics and wiring lists for each of the various HDAS units. Each Volume is broken down by system assembly, as follows:

Volume I - Assembly 1, Buffer Memory

Volume II - Assembly 2, Computer to Satellite Bus Interface and Data Formatter

Volume III - Assembly 3, Buffer Memory Controller

Volume IV - Assembly 4, Reconfigurable System Interface Unit

Volume V - Assembly 5, A/D Conversion System

VII. SOFTWARE

A general-purpose software operating system was written specifically for the SAV to provide HDAS control and data verification routines in support of system test operations. The operating system, referred to as SAVOS, is written in standard FORTRAN IV and DEC assembly language routines and executed on the PCS. SAVOS allows the user to interactively initialize and control HDAS operations along with display features to view recorded data. A complete description of the SAV software operation is contained in the following separate volumes prepared by Computer Sciences Corporation:

Volume I - System Overview

Volume II - Software Description

Volume III - SAVOS User's Guide

Volume IV - Data Tape Format

Volume V - Auxiliary Programs

APPENDIX A

SPECIFICATIONS
VERSATEC MODEL 1110A PRINTER/PLOTTER

APPENDIX A

SPECIFICATIONS
VERSATEC MODEL 1110A PRINTER/PLOTTER

Printing Specifications

Columns	132 per line
Character Spacing	12.5 per line
Line Spacing	6.6 per in.
Font	7 × 9 Dot Matrix
Speed	1000 LPM Asynchronous
Input Code	USASCII - Serial and Parallel
Character Set	64 - Standard (96 or 128 Optional)

Graphics Specifications

Plotting Width	10.24 in.
Total Writing Nibs	1024 (100 per in.)
Nib Spacing	0.010 center-to-center
Paper Drive Increment	0.010 in.
Input Parallel	1 million, ASCII characters/sec max.
Input Serial	Printer/Plotter operates asynchronously in a receive-only mode and is pin and voltage level compatible with RS-232C standard. Either 10- or 11-bit code is accepted. Recommended operating rates are 600, 1200, 2400, 4800, or 9600 bits/sec.
Plotting Speed	2.4 in./sec

General Specifications

Writing Method	Electrostatic
Paper Drive	Incremental
Paper Advance Speed	2.4 in./sec
Manual Controls, Switches, and Indicators:	
Printer/Plotter Switch Panel	Illuminated power on-off Paper advance Illuminated out-of-paper indicator Form feed

General Specifications (Concluded)

Manual Controls, Switches, and Indicators (Concluded):

Frame Mounted	Contrast Master reset
Power Required	115 VAC ± 10% 48 to 62 Hz, 800 W maximum
Size	19-in. width × 18-in. depth × 38-in. height
Net Weight	160 lb
Paper Width	11 in.
Paper Length	500-foot roll or 100-sheet fanfold
Toner Supply	2-gal disposable bottle
Concentrate	8-oz disposable bottle
Environment	Temperature: 32°F to 105°F Humidity: 10% to 95% relative humidity (non-condensing)

APPENDIX B.

MAGNETIC TAPE SYSTEM PERFORMANCE SPECIFICATIONS
MODEL 6250-66

APPENDIX B

MAGNETIC TAPE SYSTEM PERFORMANCE SPECIFICATIONS
MODEL 6250-66

Tape Speed (in./sec)	125
Density (bits/in.)	1600/6250
Recording Format	PE/GCR
Number of Tracks	9
Data Transfer Rate (kb/sec)	200 PE 781 GCR
Interblock Gap (in.)	0.6 PE/0.3 GCR
Start/Stop Time (ms)	1.1 PE/0.1 GCR
Start/Stop Distance (in.)	0.065 PE/0.016 GCR
Rewind Time, 240C-ft reel (sec)	60 ±10%
Rewind Speed (in./sec)	500
Environmental	
Operating Temperature	40°F-110°F
Relative Humidity	30%-80% non-condensing
Operating Altitude (ft)	0-4000 (0-7000 optional)
Physical	
Mounting (in.)	19 EIA Rack
Weight (lb)	300
Height (in.)	24.5
Width (in.)	19
Depth (in.)	22.5
Power	115 VAC 60Hz
Power Consumption (W)	Ready/on-line, tape loaded 1000 Operating with tape motion 1440

APPENDIX C.

AR11 A/D CONVERTER SPECIFICATIONS

APPENDIX C

AR11 A/D CONVERTER SPECIFICATIONS

Input Voltage Range	0 to +5 V -2.5 to +2.5 V (Program Selectable)	
Resolution	10 bits (1 part in 1024)	
Accuracy at 25°C	0.1% of full scale	
Number of Channels	16 (single-ended)	
Switching	Break before make	
Linearity	1/2 LSB (0.025% of full scale)	
Differential Linearity	Guaranteed: No skipped states; 95% of states ±1/2 LSB Typical: 99% of states ±1/2 LSB; 85% of states ±1/4 LSB	
Throughput Time		
Programmed Start	Multiplexer Sample-and-Hold	8 us typical
	Clock Synchronization	0-2
	Hold Delay	2
	Conversion	20
		30-32 us
Single-channel External or Clock Start	Clock Synchronization	0-2 us
	Hold Delay	2
	Conversion	20
	Sample-and-Hold reacquisition	4
		26-28 us
Throughput Rate	PDP-11/10 with optimal coding:	
Programmed Start	30 kHz	
Overflow or External Start	35 kHz	
Input Impedance	10M min., $-5\ V < V_{in.} < +5\ V$	
Input Bias Current	100 nA max., unselected channel -2 μA max., selected channel	$-5V<V_{in}<+5V$
Sample-and-Hold Tracking	Small signal bandwidth: 700 kHz Large signal slew rate limit: 1 V/us	
Sample-and-Hold Aperture	100 ns max. delay 1 ns jitter	

A/D Specifications (Concluded)

Repeatability	**rms noise 1/4 LSB maximum 1/5 LSB typical**
Crosstalk	**80 dB at 1 kHz, rolling off at 20 dB per decade**
Tamperature Stability	**Gain: 50 ppm/°C max. (20°C/LSB) Linearity: 25 ppm/°C max. (40°C/LSB)**
Warmup Time	**5 min**
Control	**Controlled by programmed instructions, clock counter overflow, or external input**
Output Format	**Parallel, 10 bits, right-justified, off-set binary, double buffered**

APPENDIX D.

SATELLITE BUS SIGNAL DEFINITION

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SATELLITE BUS SIGNAL DEFINITION

GROUP I - DATA

Data IN/OUT (32) (BUSDXX)	-	Bi-directional lines for transmission of data between devices on satellite bus.

GROUP II - CONTROL

Address (7) (BUSADXX)	-	Uni-directional lines allowing addressing of various registers in each device on the bus by the controlling computer. Of the 7 bits, 3 MSBs select one of 8 devices, while the remaining 4 select 1 of 16 registers.
Initial (BUSINIT)	-	Uni-directional pulsed signal derived from the PDP-11 reset signal. This signal is generated when the START button on PDP is depressed or a software RESET is given.
Start (BUSSTART)	-	Uni-directional pulsed signal generated by controlling computer to start bus operations between the designated master and slave devices. 5 μsec width.
In/Out (BUSINOUT)	-	Uni-directional level controlling direction of data transfers from the PDP-11 to slave. A high level (+3 V) indicates output from PDP and a low level (0.8 V) indicates input to PDP.
Read Strobe (BUSRDSB)	-	Bi-directional pulsed signal from bus master to slave indicating a read request from an addressed register. This signal is used primarily when the PDP is reading from a bus device. The width of this signal is approximately 5 μsec.
Bus Request (BUSRQST)	-	Uni-directional pulsed signal generated by PDP to bus devices for gaining bus control without destroying the contents of device registers. 5 μsec width.
Data Strobe (BUSDTSB)	-	Bi-directional pulsed signal from master to slave for strobing data into slave device. During reading operations with PDP, this signal indicates data has been accepted by PDP. The signal width will vary depending on operation. When PDP is controlling device, this signal indicates valid data from the DR11-M.

GROUP II - CONTROL (Concluded)

Data Request (BUSDTRQ)	-	Bi-directional level from slave to master notifying master that slave is ready for another burst of data. Not used when PDP-11 is master.
Finished (BUSFINS)	-	Uni-directional level from master to PDP-11 indicating bus transfers have been completed and re-initialization is necessary.

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